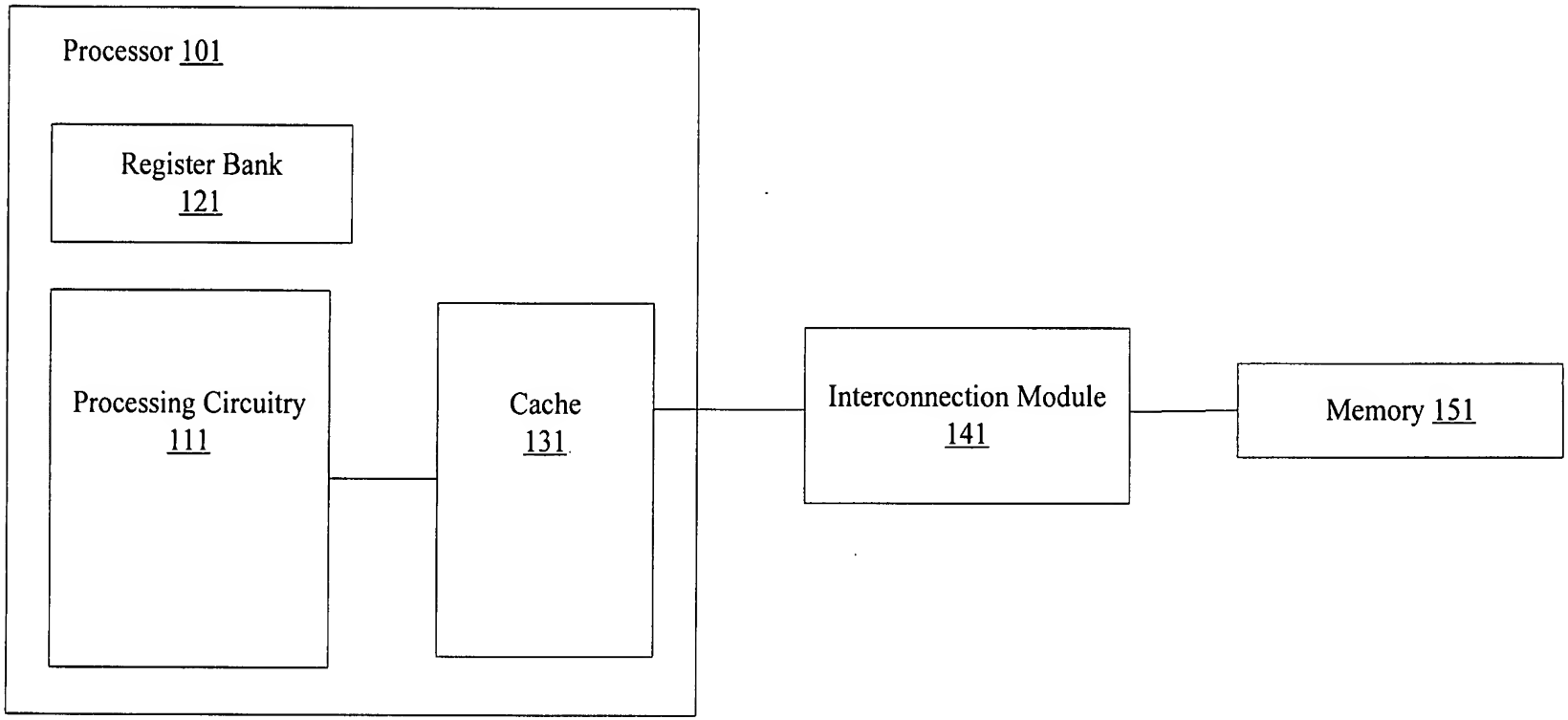

Processor 101
Register Bank
121
Processing Circuitry
111
Cache
131
Interconnection Module
141
Memory 151

Figure 1

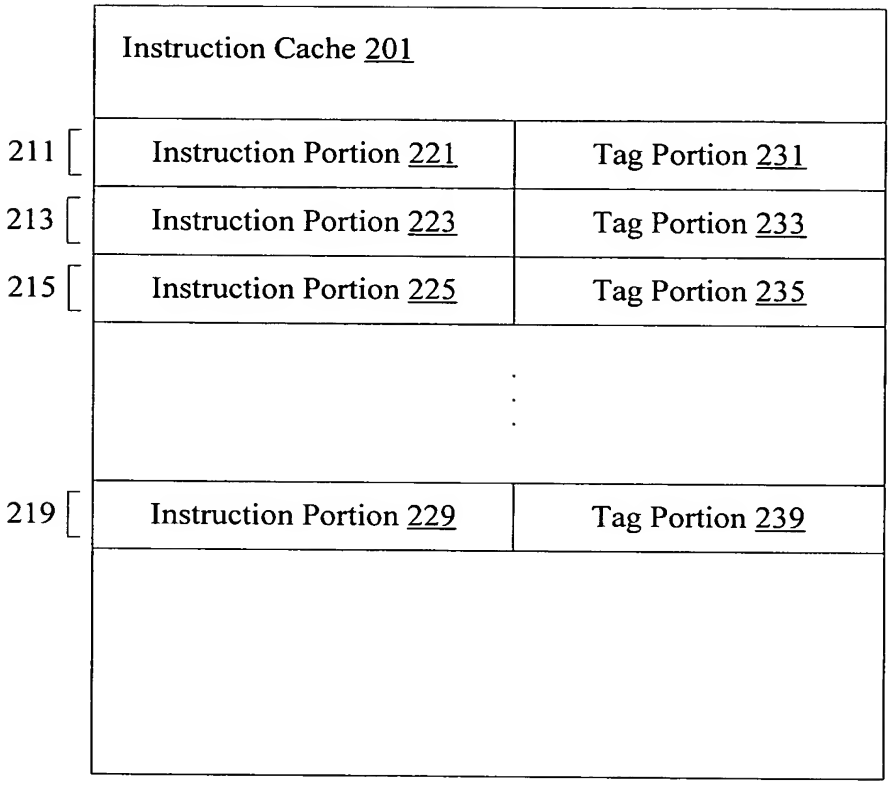

Instruction Cache 201
211
Instruction Portion 221
Tag Portion 231
213
Instruction Portion 223
Tag Portion 233
215
Instruction Portion 225
Tag Portion 235
219
Instruction Portion 229
Tag Portion 239

Figure 2

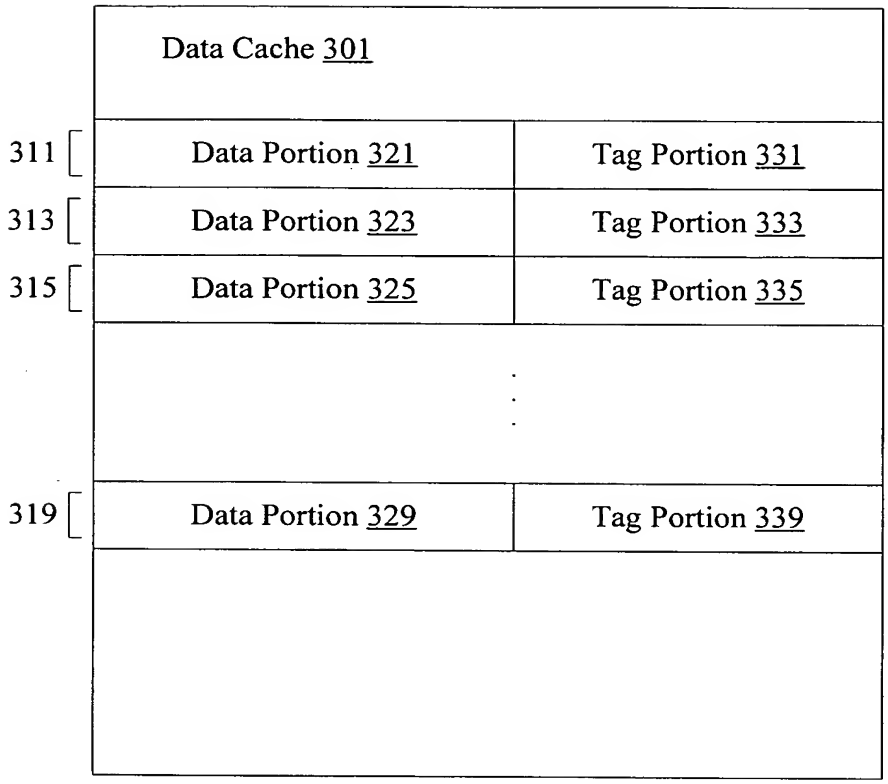

Data Cache 301
311
Data Portion 321
Tag Portion 331
313
Data Portion 323
Tag Portion 333
315
Data Portion 325
Tag Portion 335
319
Data Portion 329
Tag Portion 339

Figure 3

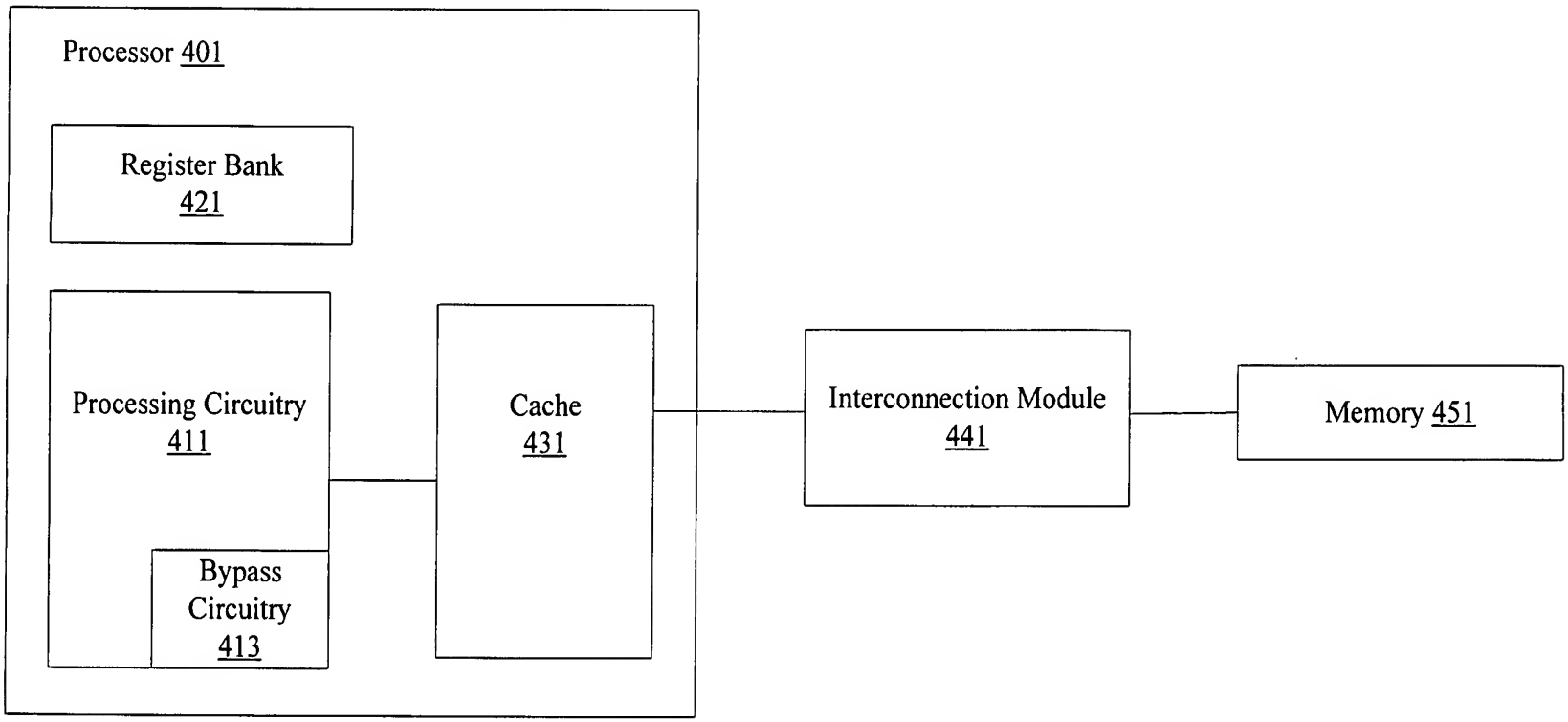

Processor 401
Register Bank
421
Processing Circuitry
411
Bypass
Circuitry
413
Cache
431
Interconnection Module
441
Memory 451

Figure 4

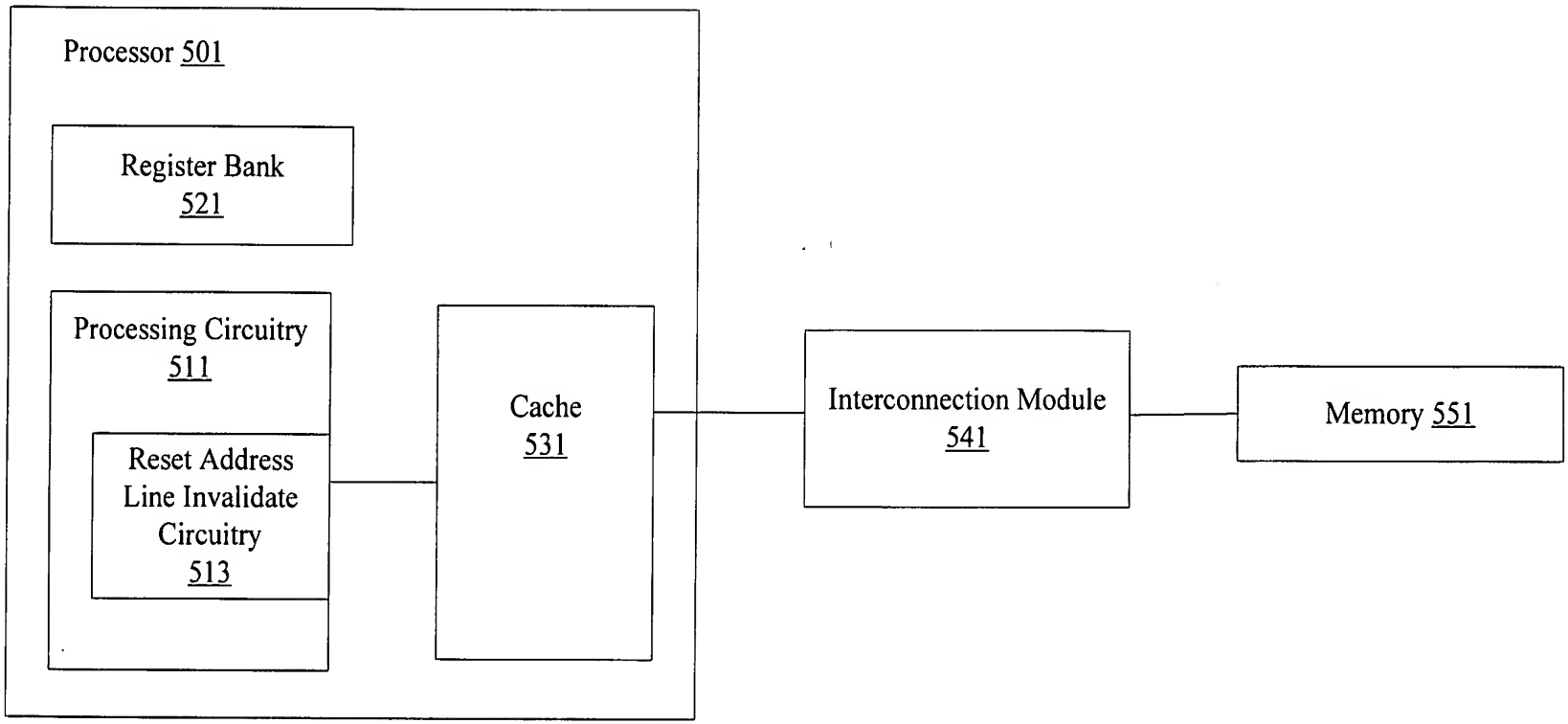

Processor 501
Register Bank
521
Processing Circuitry
511
Reset Address
Line Invalidate
Circuitry
513
Cache
531
Interconnection Module
541
Memory 551

Figure 5

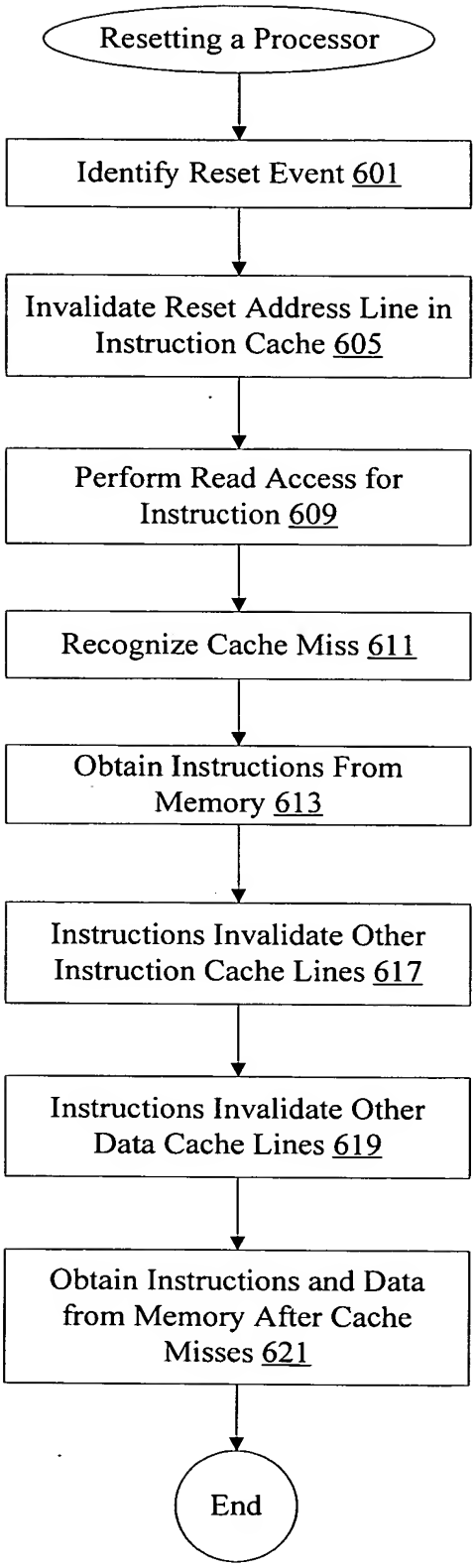

Resetting a Processor
Identify Reset Event 601
Invalidate Reset Address Line in Instruction Cache 605
Perform Read Access for Instruction 609
Recognize Cache Miss 611
Obtain Instructions From Memory 613
Instructions Invalidate Other Instruction Cache Lines 617
Instructions Invalidate Other Data Cache Lines 619
Obtain Instructions and Data from Memory After Cache Misses 621
End

Figure 6

Figure 7

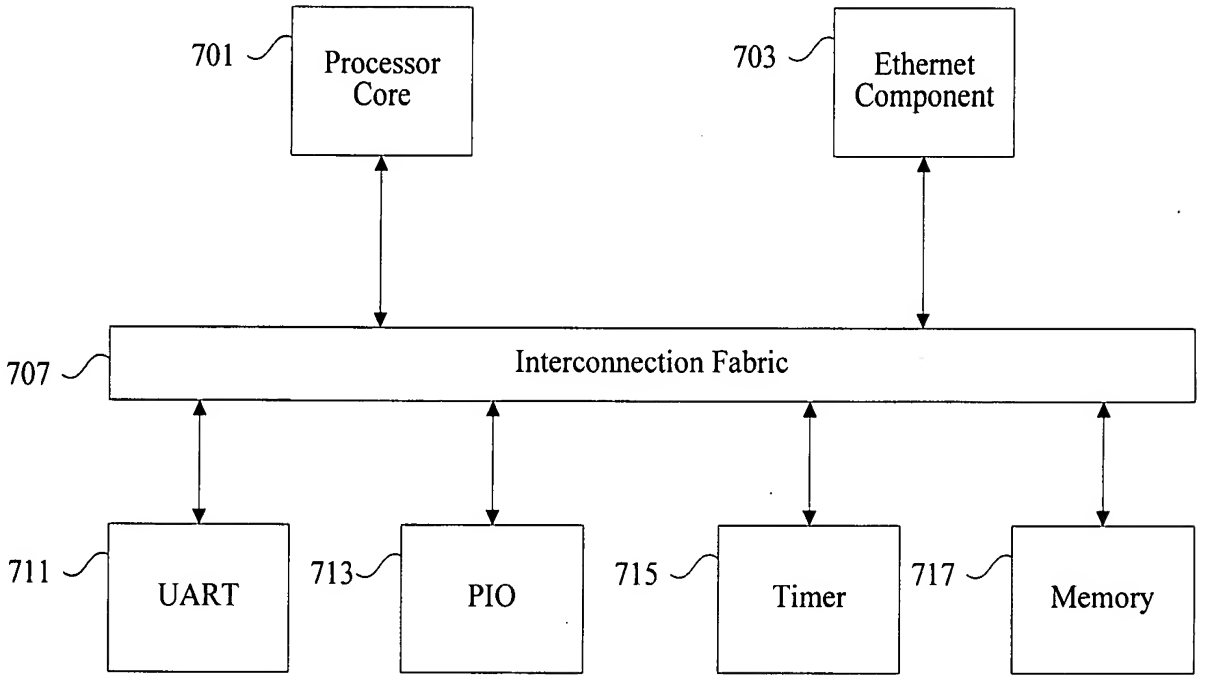
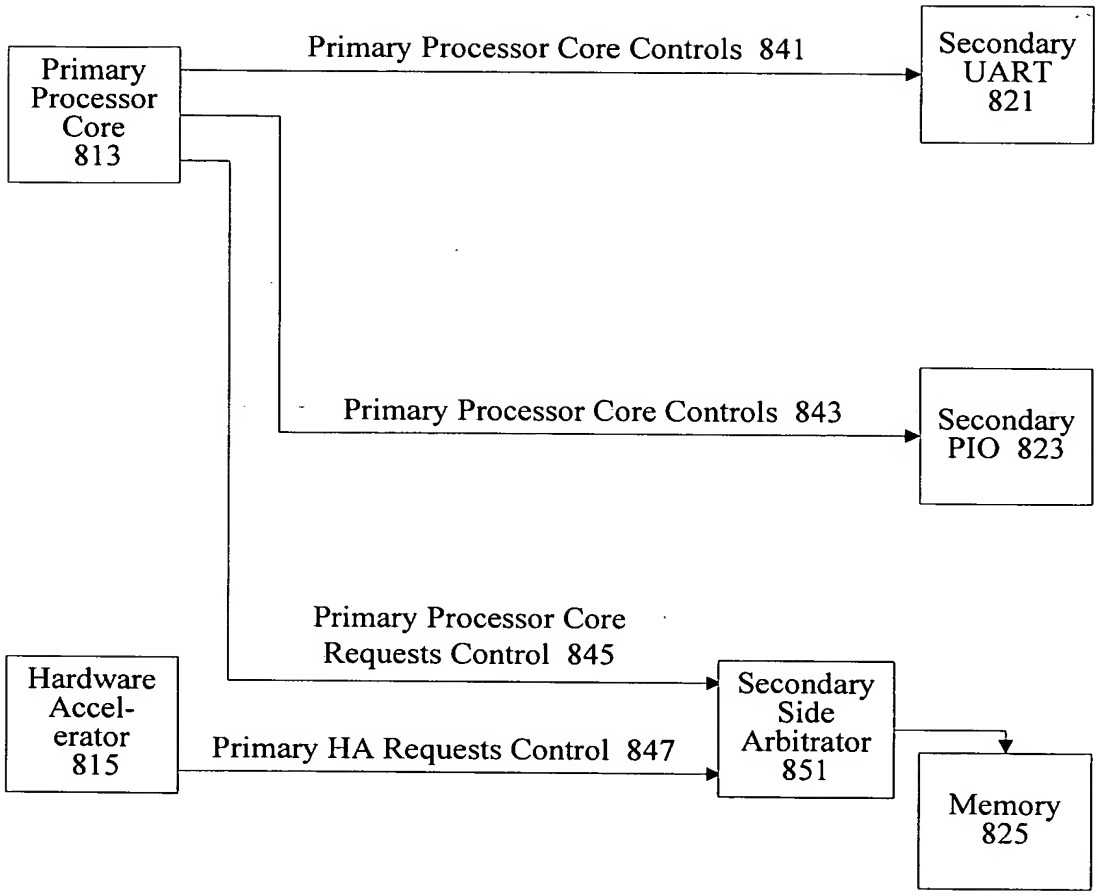

701
Processor Core
703
Ethernet Component
707
Interconnection Fabric
711
UART
713
PIO
715
Timer
717
Memory

Figure 8


Primary Processor Core 813
Primary Processor Core Controls 841
Secondary UART 821
Primary Processor Core Controls 843
Secondary PIO 823
Primary Processor Core Requests Control 845
Hardware Accel-erator 815
Primary HA Requests Control 847
Secondary Side Arbitrator 851
Memory 825

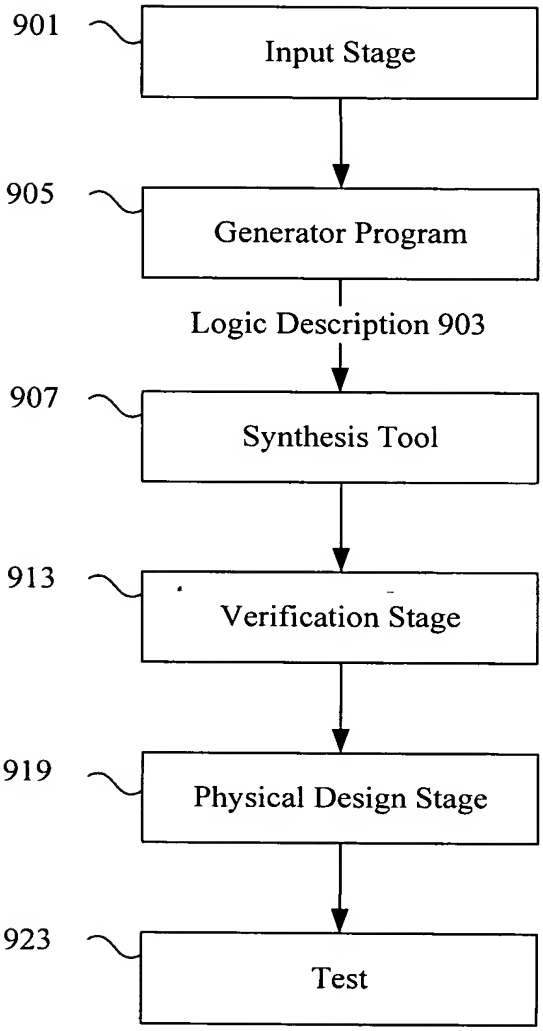

901
Input Stage
905
Generator Program
Logic Description 903
907
Synthesis Tool
913
Verification Stage
919
Physical Design Stage
923
Test

Figure 9

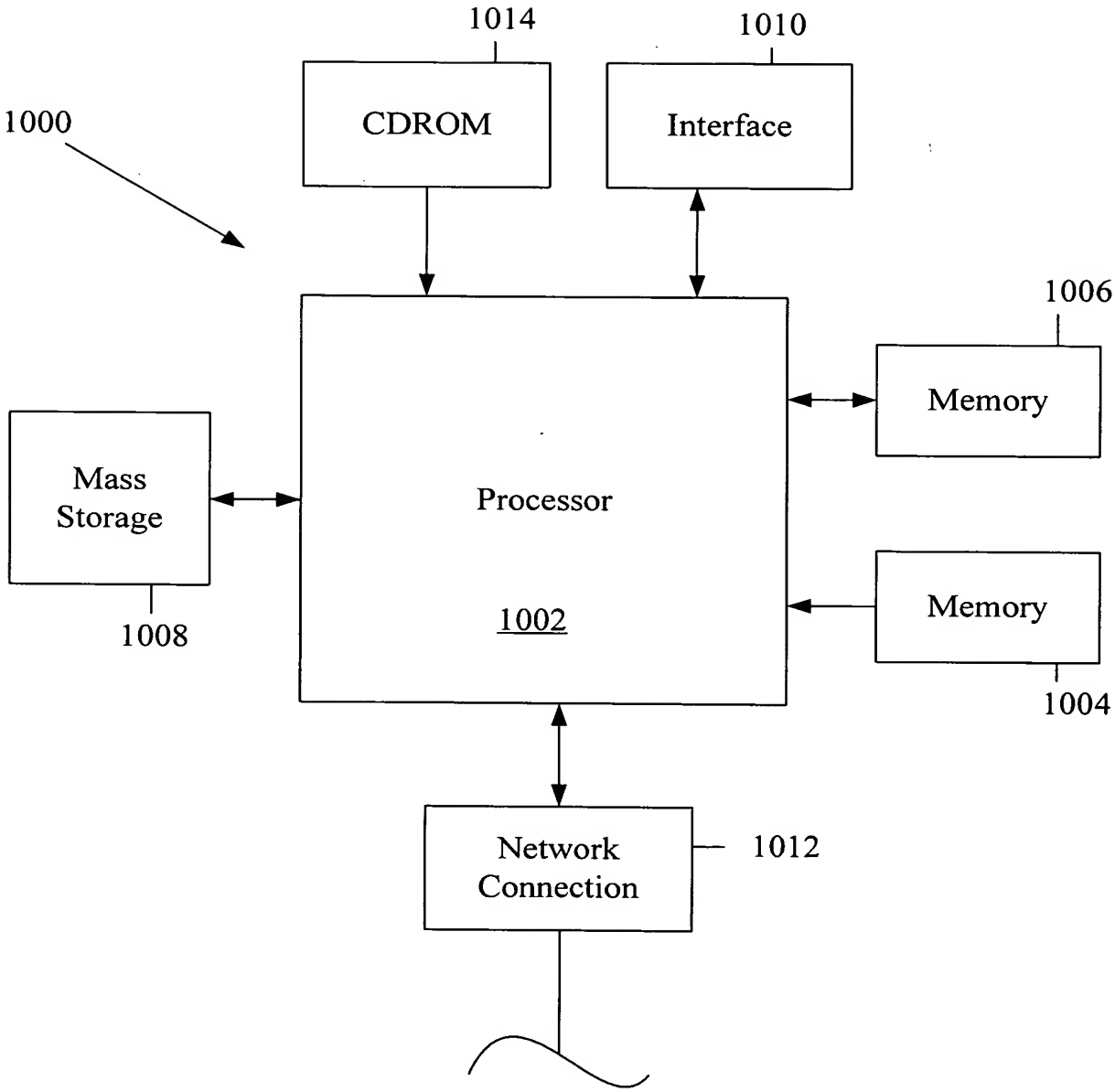

1014
1010
1000
CDROM
Interface
1006
Memory
Mass
Storage
Processor
1002
Memory
1008
1004
Network
Connection
1012

Figure 10